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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,400	04/15/2004	Michael J. Walk	P18287	8164
28062	7590	08/11/2005	EXAMINER	
BUCKLEY, MASCHOFF, TALWALKAR LLC			ANDUJAR, LEONARDO	
5 ELM STREET			ART UNIT	
NEW CANAAN, CT 06840			PAPER NUMBER	
			2826	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/825,400	WALK ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 April 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7, 10-13, 16-20, 23 and 24 is/are rejected.
- 7) ☒ Claim(s) 6,8,9,14,15,21 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of vias according to claim 6, double data rate memory according to claim 18 and the mother board coupled to the microprocessor and the memory according to claim 24 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Regarding claim 2, Chance shows an integrated circuit die 52 coupled to the interposer.

6. Regarding claim 3, Chance shows that the capacitive layer is disposed between the interposer and the integrated circuit die.
7. Regarding claim 4, Chance shows a plurality of solder columns 64 to coupled the interposer to the substrate.
8. Regarding claim 5, Chance shows that the layer material defining opening to pass the plurality of solder columns
9. Regarding claim 7, Chance shows that the layer of material is laminated to the substrate.
10. Regarding claim 10, Chance shows that a first side of the interposer is coupled to the layer of material and the capacitor is coupled to a second side of the interposer.
11. Regarding claim 11, Chen (e.g. fig. 1 and 2) shows a method comprising: fabricating a coreless substrate 54; attaching a layer of material 60 (e.g. polyimide) to the substrate, the layer of material having a lower elastic modulus than the substrate (e.g. ceramic); and coupling an interposer 92 having a capacitive layer 58 to the layer of material (col. 1/lls. 15-26; col. 4/lls. 11-22 & col. 5/lls. 57-61).
12. Regarding claim 12, Chance shows the step of fabricating solder columns 64.
13. Regarding claim 13, Chance shows the step of coupling the interposer to the solder columns.
14. Regarding claim 16, Chance shows the step of coupling an integrated circuit die 52 to the interposer.
15. Regarding claim 17, Chance shows that step of coupling the integrated circuit die to the capacitive layer.

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 18-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chance et al. (US 5,177,594).

18. Regarding claim 18, Chance shows (e.g. fig. 1 and 2) as system comprising: a first semiconductor chip 52, a coreless substrate 54; a layer of material attached to the substrate 60 (e.g. polyimide), the layer of material having a lower elastic modulus than the substrate (e.g.. ceramic); an interposer 92 coupled to the layer of material; a capacitive layer 58 coupled to the interposer and a second semiconductor chip 52 coupled to the first chip (col. 1/lls. 15-26; col. 4/lls. 11-22 & col. 5/lls. 57-61). Chance does not teach that the first semiconductor chip is a microprocessor and the second semiconductor chip is a double data rate memory. Nevertheless, this type of description is considered to be an intended use of the first and second semiconductor chips. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the

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prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

19. Regarding claim 19, Chance shows an integrated circuit die 52 coupled to the interposer.

20. Regarding claim 20, Chance shows that the capacitive layer is disposed between the interposer and the integrated circuit die.

21. Regarding claim 23, Chance shows a first side of the interposer is coupled to the layer of material and the capacitor is coupled to a second side of the interposer.

22. Claims 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chance et al. (US 5,177,594) in view of Fritz (US 6,734,540).

23. Regarding claim 24, Chance shows most aspects to the instant invention including a first and second chip (i.e. microprocessor & memory) electrically coupled to the substrate. Chance does not show that the substrate is electrically coupled to a next packaging integration level to interconnect the different semiconductor assemblies with other elements of the electronic system. Note that a semiconductor package by itself does not have any practical use unless it is interconnected with another system unit. For example, Fritz (e.g. fig. 5) teaches a substrate 540 connected to a motherboard 550. It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically and physically couple the device disclosed by Chance to a motherboard as suggested by Fritz to interconnect the device with other elements of the electronic system and to provide a heat transfer means or mechanical support.

***Allowable Subject Matter***


24. Claims 6, 8, 9, 14, 15, 21 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Leonardo Andújar  
Patent Examiner  
Art Unit 2826  
